REMARKS

Claims 1-25 are pending in the above-identified application. Claim 1 is independent.

The examiner rejected claims 1 and 3-12 under 35 U.S.C. §102(e) as being anticipated by U.S. Publication No. 2002/0076936 to Iguchi. The examiner further rejected claims 2 and 14-25 under 35 U.S.C. §103(a) as being unpatentable over Iguchi in view of U.S. Patent No. 6,335,218 to Ota et al., and further in view of U.S. Patent No. 6,008,539 to Shibata et al.

Specifically, with respect to independent claim 1, the examiner stated:

> Iguchi discloses a semiconductor device with
> (1) providing a semiconductor body containing a substrate (1) and at least one nitride compound semiconductor disposed on the substrate (1) (see Figure 22);
> applying a metal layer to a surface of the semiconductor body (see Figure 22);
> dry-chemically removing a part of the metal layer and a part of the semiconductor body previously covered by the removed metal layer (see paragraphs [0184]-[0188]. Figures 22-23); (Office Action, pages 2-3)

Applicant respectfully disagrees with the examiner's characterization of Iguchi.

Applicant's independent claim 1 discloses a method for fabricating a semiconductor component that includes the feature of "providing a semiconductor body containing a substrate and at least one nitride compound semiconductor disposed on the substrate."

Iguchi describes a method for fabricating a semiconductor IC, particularly IC's used as capacitance devices, in which an IrO_2 film is patterned by dry etching using a resist mask (see the Abstract, and paragraphs 1 and 12). Iguchi's explains that:

> **[0176] Initially, a field oxide film 30 for device isolation and a p type well 3 are formed on a main plane of a semiconductor substrate (wafer) 1 made of single crystal silicon having a p type conductivity and resistivity of about 10 Ωcm as shown in FIG. 20. A field oxide film 30 is formed by a known LOCOS process. The p type well 3 is formed by ion-implanting n type impurity ions such as P (phosphorus) and then annealing the semiconductor substrate 1 to thermally diffuse the impurity.**
>
> **[0177] After the surface of the p type well 3 is washed with an HF (hydrofluoric acid)-based washing solution, the semiconductor substrate 1 is wet oxidized to form a clean gate oxide film 5 is formed on the p type well 3. After a gate electrode 6 is formed subsequently over the gate oxide film 5, an n type impurity such as P (phosphorus) is ion-implanted to form an n type semiconductor region 7 (source and drain). (emphasis added, page 9, paragraphs 176-177)**

Thus, the semiconductor material of Iguchi's semiconductor IC is silicon-based.

Iguchi further describes that a silicon nitride film 35 is deposited over a silicon oxide film 31 (see FIG. 22 and paragraph 179). Iguchi further explains that "the silicon nitride film 35 is used as an oxidation-resistant barrier layer to prevent the plugs 34 inside the contact holes 32 and 33 made of the W film from being oxidized and increasing its thickness during annealing of the PZT film 38A" (paragraph 180). Thus, Iguchi's silicon nitride film (whose chemical representation is Si_3N_4) is not a compound semiconductor, but an insulator. Indeed, as described, for example, on page 504 of S. M. Sze's "Physics of Semiconductor Devices" (Second Edition, John Wiley & Sons):

> **Among several kinds of MIOS (metal-insulator-SiO_2-Si) memory devices, the MNOS (metal Si_3N_4-SiO_2-Si) device is the most popular. Other MIOS devices use different insulators to replace the silicon nitride film such as aluminum oxide, tantalum oxide, and titanium oxide.**

(A copy of the excerpt from the above-identified Sze reference is attached herewith for the examiner's convenience.)

The only other material used in Iguchi's device that contains nitride is the titanium nitride (TiN) film 36. Iguchi describes that after the silicon nitride is deposited on the silicon oxide film 31, "[a]n about 20 nm-thick TiN film 36, an about 175 nm-thick Pt film 37A, an about 250 nm-thick PZT film 38A and an about 175 nm-thick IrO_2 film 39A are then deposited serially by sputtering over the silicon nitride film 35" (pages 9-10, paragraph 179). Iguchi then explains that "[t]he TiN film 36 is used as a barrier metal for preventing diffusion of Pb in the PZT film 38A and for improving adhesion power of the interface between the Pt film 37A and the silicon nitride film 35" (Page 10, paragraph 180). Thus, the TiN film is a metal used as a barrier for preventing diffusion of lead. The TiN film, therefore, is not a semiconductor compound.

Accordingly, Iguchi does not disclose a nitride compound semiconductor, and therefore Iguchi neither discloses nor suggests at least the feature of "providing a semiconductor body containing a substrate and at least one nitride compound semiconductor disposed on the substrate," as required by applicant's independent claim 1.

Furthermore, applicant's independent claim 1 recites "applying a metal layer to a surface of the semiconductor body; and dry-chemically removing a part of the metal layer and a part of the semiconductor body previously covered by the removed metal layer."

Particularly, as explained in the specification of the above-identified application:

> **The method has the advantage that a metal layer is applied to the semiconductor body as early as before the patterning, which metal layer may subsequently serve as a contact layer or as part of a contact layer.**
>
> **The method is particularly preferably used for fabricating a low-resistance p-type contact, a self-aligning bottommost p-type contact layer, and preferably at the same time, a dielectric etching auxiliary mask applied above the p-type contact being used. A p-type connection layer (e.g. connection metallization) is applied before the etching of the semiconductor material and both the underlying p-type contact layer and the p-type nitride semiconductor layer are patterned chemically, in particular dry chemically, in one (or more) successive method steps. (Specification, page 5, line 21, to page 6, line 11)**

The specification further describes:

> **With the method, the entire surface of a p-type nitride semiconductor structure that is available for electrical connection is completely metallized in conjunction with very steep sidewalls of the p-type nitride semiconductor. (Specification, page 7, lines 4-7)**

Thus, by dry chemically removing part of the semiconductor body and the metal layer that has previously been applied to the semiconductor body, the surface of the semiconductor body that is available for electrical connection is covered with a metal contact. Furthermore, by applying the metal layer to the semiconductor body before the patterning is performed, low contact resistance is achieved (see Specification, page 7, line 24, to page 8, line 2).

In contrast, Iguchi explains:

> **[184] Next, the photoresist film formed on the IrO_2 film 39A is patterned to form a resist mask 40 as shown in FIG. 23. The IrO_2 film 39A is dry etched with this resist mask 40 as the mask, forming the top electrode 39 of the information storage capacitance device C. The etching method of Embodiment 1, that uses the etching gas comprising the chlorine gas as the main component and containing oxygen as the additional gas, is used at this time, and a pattern can be obtained in which the side wall adhesion film hardly adheres to the resist mask 40 and to the side surface of the IrO_2 film 39A (top electrode). In consequence, pattern accuracy of the top electrode 39 can be improved, and over-etching and washing for removing the side wall adhesion film become unnecessary.**

[0185] Next, after the resist mask 40 is removed by ashing, the photoresist film formed on the top electrode 39 is patterned to form a resist mask 41 as shown in FIG. 24. The PZT film 38A, the Pt film 37A and the TiN film 36 are dry etched with this resist mask 41 as the mask. The process steps described so far provides the information storage capacitance device C having the bottom electrode 37 comprising the Pt film 37A, the capacitance insulation film 38 comprising the PZT film 38A and the top electrode 39 comprising the IrO_2 film 39A. In this way, the FeRAM comprising the memory cell selection MISFETQs and the information storage capacitance device C connected in series with the MISFETQs is completed. (Iguchi, page 10, paragraphs 184-185).

Thus, only the materials disposed above the silicon nitride film (which as previously explained, does not form part of the semiconductor compound) are dry-etched. The semiconductor body itself is not dry-etched. Accordingly, Iguchi does not disclose or suggest at least the feature of "dry-chemically removing a part of the metal layer and a part of the semiconductor body previously covered by the removed metal layer," as required by applicant's independent claim 1.

Because Iguchi does not disclose or suggest at least the features of "providing a semiconductor body containing a substrate and at least one nitride compound semiconductor disposed on the substrate" and/or "dry-chemically removing a part of the metal layer and a part of the semiconductor body previously covered by the removed metal layer," applicant's independent claim 1 is therefore patentable over the cited art.

Claims 2-25 depend from independent claim 1 and are therefore patentable for at least the same reasons as applicant's independent claim 1.

It is believed that all the rejections and/or objections raised by the examiner have been addressed.

In view of the foregoing, applicant respectfully submits that the application is in condition for allowance and such action is respectfully requested at the Examiner's earliest convenience.

All of the dependent claims are patentable for at least the reasons for which the claims on which they depend are patentable.

Canceled claims, if any, have been canceled without prejudice or disclaimer.

Any circumstance in which the applicant has (a) addressed certain comments of the examiner does not mean that the applicant concedes other comments of the examiner, (b) made arguments for the patentability of some claims does not mean that there are not other good reasons for patentability of those claims and other claims, or (c) amended or canceled a claim does not mean that the applicant concedes any of the examiner's positions with respect to that claim or other claims.

No fees are believed due. Please apply any charges to deposit account 06-1050, referencing attorney docket 12406-140001.

Respectfully submitted,

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